ABSTRACT OF THE DISCLOSURE

An apparatus and method are provided that enable a multiple instruction set architecture (ISA) central processing unit (CPU) to distinguish between different program instructions corresponding to different ISAs during execution of a multiple-ISA application program. The apparatus allows the multiple-ISA CPU to select a particular ISA decoding mode corresponding to a program instruction. The program instruction is located at an address within an address space of the multiple-ISA CPU. The apparatus includes a plurality of boundary address registers and ISA mode selection logic. The plurality of boundary address registers can be dynamically loaded to partition the address space into a plurality of address ranges, where each of the plurality of address ranges corresponds to each of a plurality of ISA decoding modes. The ISA mode selection logic is coupled to the plurality of boundary address registers. The ISA mode selection logic receives the particular address, and compares it against the plurality of address ranges to determine the particular ISA decoding mode for the particular program instruction.